In the Specification

Please amend the title shown on page 1 of the specification as follows:

~~A 6F^2 DRAM Array, A DRAM Array Formed On A Semiconductive Substrate,~~ A Method Of Forming Memory Cells ~~In A 6F^2 DRAM Array~~ And A Method Of Isolating A Single Row Of Memory Cells ~~In A 6F^2 DRAM Array~~

Please amend the "Cross Reference to Related Application" on page 1, after the Title, as follows:

This patent application is a Division of U.S. Patent Application Serial No. 10/280,757, (now U.S. Patent No. _____) filed October ~~21~~, 24, 2002, entitled "A 6F^2 DRAM Array, A DRAM Array Formed On A Semiconductive Substrate, A Method Of Forming Memory Cells In A 6F^2 DRAM Array And A Method Of Isolating A Single Row Of Memory Cells In A 6F^2 DRAM Array", naming Luan Tran as inventor, which in turn was a Division of U.S. Patent Application Serial No. 09/810,933, filed March 16, 2001, now U.S. Patent No. 6,545,904, the ~~disclosure~~ disclosures of which ~~is hereby~~ are incorporated herein by reference.

Please amend the second paragraph at page 12 of the application as follows:

At the far left of Fig. 3, a first diffusion region 72 is shown that is coupled to one of the ~~bit line~~ bitline contacts 60. In one embodiment, the bitline contact 60 is formed from conventional polysilicon and is insulated from laterally adjacent structures by a conventional dielectric 74.

Please amend the first paragraph at page 16 of the application as follows:

In a step S3, a second gate dielectric growth process is carried out to form the first gate dielectrics 76, 90 for the access devices 14. The step S3 may increase the thickness of the initial dielectric in the first regions to provide the thicker second dielectric 86 of Fig. 3. In one embodiment, the gate dielectrics 76, 86 and 90 comprise silicon dioxide ~~gown~~ grown via conventional oxidation processes. The process P1 then ends, and other processing is carried out to form the completed DRAM.